# PATENT ABSTRACTS OF JAPAN

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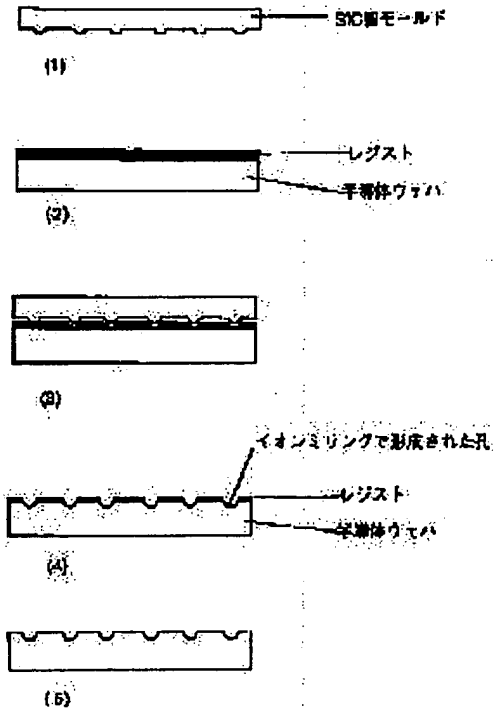
## (54) FORMATION METHOD FOR FINE PATTERN OF SEMICONDUCTOR SURFACE

(57)Abstract:

PROBLEM TO BE SOLVED: To form a fine pattern on a semiconductor surface by pressing a mold on which a projected-and-recessed pattern is formed against a resist film of the semiconductor surface to transfer a projected-and-recessed reverse pattern to the surface of resist film, and then working the resist film and the semiconductor surface under it in the dry etching method of low material selectivity.

SOLUTION: A mold on which projected-and-recessed type pattern is formed is prepared, then resist is applied to a semiconductor surface, and the mold is pressed against the applied resist film to transfer the projected-and-recessed pattern. At this time, by applying proper pressure, a faithfully patterned recessed part is formed after a formation of the projected part of the mold on the resist film. Then the resist film and the semiconductor surface under it are etched in the dry etching method of low material selectivity while maintaining a projected-and-recessed reverse form of the mold cut into the resist film. As a result, a fine pattern is formed on the semiconductor surface.



LEGAL STATUS

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| [Date of request for examination] | 23.01.2001 |
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* NOTICES *



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CLAIMS

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[Claim(s)]
[Claim 1] the 1st process which imprints the concavo-convex reverse pattern of this pattern on this resist film front face by forcing the mold in_which the pattern of a concavo-convex mold was formed on the resist film formed in the semi-conductor front face -- this -- the detailed pattern-formation approach on the front face of a semi-conductor characterized by to consist of this resist film after the 1st process, and the 2nd process which processes the semi-conductor front face under it by the low dry-etching method of ingredient selectivity.
[Claim 2] The 1st process which imprints the concavo-convex reverse pattern of this pattern on this resist film front face by forcing the mold in which the pattern of a concavo-convex mold was formed on the resist film formed in the semi-conductor front face, this -- with this resist film after the 1st process, and the 2nd process which processes the semi-conductor front face under it by the low dry etching method of ingredient selectivity this -- the detailed pattern formation approach on the front face of a semi-conductor characterized by consisting of the 3rd process which carries out etching processing of the semi-conductor front face after the 2nd process by the wet etching method.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the detailed pattern formation approach on the front face of a semi-conductor.
[0002]
[Description of the Prior Art] Formation of a detailed pattern on a semi-conductor front face is important when producing the semiconductor device which used the quantum effectiveness. The range of the pattern dimension which the quantum effectiveness discovers is several [ about ] nm to dozens of nm. Since this dimension range is dimension range comparable as the wavelength of light, it is difficult the range to process it using photolithography. Although EB lithography which exposes the resist film with an electron ray is used for processing of this dimension range instead of photolithography, there is a problem that a throughput (throughput per time amount) is small in this approach. Generally a "resist" means the paint film ingredient which has etching-proof nature here.
[0003] Recently, the nano imprint method is used as a technique replaced with photolithography or EB lithography (S. Y.Chou, et.al., Science, vol.272, p.85-87, 5 April, 1996 reference). This approach is an approach of using as a mask the resist which formed the pattern of an indentation and formed the pattern of an indentation, and processing a semi-conductor front face, by forcing the mold made from SiO2 (mold) which formed the pattern beforehand on the resist applied to the semi-conductor front face.
[0004] Drawing 8 is a sectional view explaining the process of detailed pattern formation of having used this approach. It consists of the following six processes.
[0005] Drawing 8 (1) - (6) corresponds to a process 6 from the following process 1, respectively.
[0006] [Process 1] The mold made from SiO2 in which the convex type pattern was formed is prepared.
[0007] [Process 2] A resist is applied to the front face of a semi-conductor wafer.
[0008] [Process 3] The mold made from SiO2 is forced on a resist by the pressure of about 1.3x107Pa, and the pattern of an indentation is imprinted.
[0009] [Process 4] The resist in which the indentation was formed is processed by oxygen use reactive ion etching (oxygen RIE).
[0010] [Process 5] A resist is used as a mask and a semi-conductor front face is etched.
[0011] [Process 6] A resist is removed.
[0012]
[Problem(s) to be Solved by the Invention] A detailed pattern is formed in a semi-conductor front face through the above processes. In this technique, in order to imprint a pattern to the resist applied to the semi-conductor front face, the process which applies a resist, the process which processes the resist in which the indentation was formed, with Oxygen RIE, and the process which removes a resist are required for a semi-conductor front face, and a process is complicated. Moreover, by this approach, as shown in drawing 8 (4), Oxygen RIE will remove the resist of a thin part completely. Since Oxygen RIE is the high (that is, an etch rate changes greatly with classes of ingredient) etching approach of ingredient selectivity, although a resist is etched, a semi-conductor is not etched by this approach. Therefore, there is a trouble that the pattern which consists of a configuration of the crevice reflecting the configuration of the heights currently formed in mold of Oxygen RIE cannot be imprinted on a semi-conductor front face.

[0013] The technical problem which this invention tends to solve is offering the detailed pattern formation approach on the front face of a semi-conductor which can imprint the pattern which consists of a configuration of the crevice reflecting the configuration of the heights which solve the above-mentioned trouble and are formed in mold on the surface of a semi-conductor.
[0014]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the detailed pattern-formation approach on the front face of a semi-conductor of this invention is characterize by to consist of the 1st process which imprints the concavo-convex reverse pattern of this pattern on this resist film front face, and this resist film and the 2nd process which processes the semi-conductor front face under it by the low dry etching method of ingredient selectivity by forcing the mold in which the pattern of a concavo-convex mold was formed on the resist film formed in the semi-conductor front face.
[0015] Furthermore, the detailed pattern formation approach on the front face of a semi-conductor concerning this invention The 1st process which imprints the concavo-convex reverse pattern of this pattern on this resist film front face by forcing the mold in which the pattern of a concavo-convex mold was formed on the resist film formed in the semi-conductor front face, this resist film and the 2nd process which processes the semi-conductor front face under it by the low dry etching method of ingredient selectivity -- this -- it is characterized by consisting of the 3rd process which carries out etching processing of the semi-conductor front face after the 2nd process by the wet etching method.
[0016]
[Embodiment of the Invention] The resist film which forced mold conventionally and formed the pattern was processed with Oxygen RIE. This invention differs from the conventional approach to it in the point processed by the low (that is, an etch rate does not change greatly with classes of ingredient) dry etching method of ingredient selectivity. In order to use the low dry etching method of ingredient selectivity, etching progresses so that the indentation configuration (crevice configuration) of the heights of the mold imprinted by the resist film may be maintained. In the part removed completely, a semi-conductor front face pulls, continuation etching is carried out, the detailed pattern with which the configuration of the heights of mold was reflected carries out concavo-convex reversal, and the resist film is imprinted by etching on a semi-conductor front face.
[0017] (Gestalt 1 of operation) Drawing 1 is drawing which explains the process of the detailed pattern formation approach on the front face of a semi-conductor concerning this invention about the case where the above-mentioned concavo-convex mold pattern is a convex type pattern. In addition, even if it replaces this convex type pattern by the common concavo-convex mold pattern, this invention is carried out like the gestalt of the operation explained below. The detailed pattern formation approach of this invention **** semi-conductor front face consists of the following five processes also including preparation of mold. Each process corresponds to (1) - (5) of drawing 1 , respectively.
[0018] [Process 1] The mold in which the convex type pattern was formed is prepared.
[0019] [Process 2] A resist is applied to a semi-conductor front face.
[0020] [Process 3] Mold is forced on this resist and the pattern of an indentation is imprinted.
[0021] [Process 4] It is processed by the low dry etching method of ingredient selectivity.
[0022] [Process 5] A resist is removed.
[0023] Next, it explains in more detail about each process.
[0024] First, the 1st process is explained. Mold consists of a single crystal wafer of SiC, and the pattern is formed in the front face using the usual electron beam (EB) lithography. The single crystal of SiC is used from the point of mechanical reinforcement, and the point that EB lithography can be used. This mold can be repeatedly used, once it produces. Therefore, there is an advantage that a throughput improves, compared with conventional photolithography and EB lithography. The example of the relation between the heights of mold and the configuration of the hole formed in the semi-conductor front face corresponding to it is shown in drawing 2 . (1) of drawing 2 is the example of semi-sphere-like heights, and (2) of drawing 2 is the example of conic heights, and (3) of drawing 2 R> 2 is the example of the heights of a square shape. Thus, if this invention is used, the pattern which consists of a concavo-convex reversal configuration reflecting the configuration of mold can be formed in a semi-conductor front face.
[0025] Next, the 2nd process is explained. A resist is applied to a semi-conductor front face. When mold is forced, the ingredient of this resist has the softness and fluidity with moderate extent which deform according to the pattern formed in mold, and even after it removes mold, it should have only the hardness which maintains a pattern. The

polymethylmethacrylate (PMMA) used for the resist used for photolithography or EB lithography as an example of the ingredient of a resist is mentioned.

[0026] Next, the 3rd process is explained. This process is a process which forces mold on the resist film applied to the semi-conductor front face, and imprints a pattern. The contrast (location-change of thickness) of thickness is formed in the resist film by forcing mold. By impressing a moderate pressure, the crevice configuration which modeled the configuration of the heights of mold faithfully is formed in the resist film.

[0027] Next, the 4th process is explained. An etch rate is not based on an ingredient as ingredient selectivity is low, but the almost same thing is meant. The etching method typical as such an etching method is the ion milling method. By this approach, since the etch rate of a semi-conductor is almost the same as the etch rate of a resist, while the concavo-convex reversal configuration of the mold carved to the resist film is saved, etching advances. A resist is removed for a short time and, as for the thin part of the resist film, a semi-conductor front face is etched succeedingly. And although a semi-conductor is deeply etched in the thin part of the resist film, a semi-conductor front face is not etched, or the part with the thick resist film is shallowly etched, even if etching is performed. Therefore, a pattern with the crevice corresponding to the configuration of the heights of mold is formed in a semi-conductor front face. The time amount of etching can be freely set up, if it is before the time amount by which the thick part of the resist film is removed from the time amount from which the thin part of the resist film is removed. If it etches until a resist is removed completely, the 5th following process is unnecessary.

[0028] As explained above, this invention performs etching of a resist, and etching of a semi-conductor according to one etching process. On the other hand, since the etch rate to a semi-conductor is almost zero, etching stops the oxygen RIE used for the conventional approach in the place which the semi-conductor front face exposed. Therefore, processing on the front face of a semi-conductor must have a line trap using other etching approaches.

[0029] Next, the 5th process is explained. At this process, the resist which remains on the semi-conductor front face is removed.

[0030] A detailed pattern is formed in a semi-conductor front face through the above processes.

[0031] Drawing 3 is the mimetic diagram of the semi-conductor substrate which formed the detailed pattern by the approach of this invention. (1) of drawing 3 is the perspective view of a semi-conductor substrate, and (2) of drawing 3 is the A-A' sectional view of (1) of drawing 3 . Although the example of the detailed pattern which consists of a hole was shown in drawing 3 , you may be the pattern which consists not only of this but of a linear slot. Moreover, a pattern may be a periodic pattern and may not have especially periodicity. In short, the hole and slot which caved in locally on the semi-conductor front face should just be given.

[0032] Drawing 4 shows the example of a detailed pattern. (1) of drawing 4 , (2), and (3) are the examples of the periodic pattern which consists of a hole, and they are a square pattern, the Mikata pattern, and a roppo pattern, respectively. The example of the periodic pattern which consists of a linear slot is shown in (4) of drawing 4 . One example of application of this pattern is a diffraction grating.

[0033] Moreover, drawing 5 showed the example of the configuration of a hole and, as for (2) of circular and drawing 5 , (1) of drawing 5 showed the example of a hexagon, as for (3) of a square and drawing 5 .

[0034] In this invention, in order to process it by the low dry etching method of ingredient selectivity, the configuration of a hole as shown in drawing 5 is faithfully formed in a semi-conductor substrate front face.

[0035] (Gestalt 2 of operation) The gestalt of the 2nd operation was shown in drawing 6 .

[0036] First, wet etching of the substrate was carried out by ion milling like the gestalt 1 of the above-mentioned implementation after forming the several nm periodic etching section in the front face of a GaAs substrate or an InP substrate. Since the part of a hole, i.e., the part etched by ion milling, has got an impact of ion in the case of ion milling, it has deteriorated locally. Therefore, a property differs from other parts. Therefore, the case where the part of a hole is etched alternatively, and the case where the other part is etched alternatively can be suitably chosen by choosing the class of etching reagent. (1) of drawing 6 is a sectional view at the time of etching the part of a hole using the etching reagent etched alternatively. The configuration before and behind etching is shown in drawing 6 , respectively. When etching the front face of the GaAs substrate in which the detailed pattern was formed, as an example in such a case with the -61% nitric-acid-water mixed liquor (capacity mixing ratio 1:3:10) of 50% fluoric acid, the front face of the InP substrate in which the detailed pattern was formed may be etched with the mixed liquor (capacity mixing ratio 1:9) of 36% hydrochloric-acid-water. In addition, a fluoric acid system solution can also be used for etching of an InP

substrate.
[0037] (2) of drawing 6 is a sectional view at the time of etching except the part of a hole using the etching reagent etched alternatively. It is a point which is different from the case where the point which is projecting is (1) of drawing 6 , in after the part of the hole before etching etching. As an example in such a case, the front face of the GaAs substrate in which the detailed pattern was formed may be etched with the -30% hydrogen-peroxide-water mixed liquor (capacity mixing ratio 1:1:4) liquid of 50% fluoric acid. Here, although not illustrated, semi-conductors other than this and the combination of an etching reagent can also be used. Moreover, if the configuration of the hole after etching may turn into a configuration which reflected the anisotropy of the crystal face like the square drill according to the class of etching reagent, it may become the configuration which wore the gently-sloping radius of circle.
[0038] Since it goes on even if etching meets a substrate side in etching a substrate by wet etching using the gestalt, i.e., the etching solution, of this operation, even if it does not remove a resist from a substrate side in advance, the resist film will exfoliate from a substrate side as etching advances. That is, the process which removes a resist from a substrate side before wet etching is not necessarily required in this case.
[0039] Next, the use gestalt of the semi-conductor substrate of this invention is explained.
[0040] (Gestalt of use) The use gestalt of the detailed pattern formed in drawing 7 by operation at this invention was shown. In this case, a semi-conductor front face is used as a substrate of crystal growth as it is.
[0041] In the gestalt of this use, growth equipment is loaded with the semi-conductor substrate which formed the detailed pattern like the gestalt 1 of operation as it is, and epitaxial growth is performed on this semi-conductor substrate.
[0042] Since the part of a hole, i.e., the part etched by ion milling, has got an impact of ion in the case of ion milling, it has deteriorated locally. Therefore, a property differs from other parts. Therefore, the case where it grows up to be the part of a hole alternatively, and the case where it grows up to be the other part alternatively can be suitably chosen by choosing the class of semi-conductor growing epitaxially.
[0043] The case where it grew epitaxially into the part of a hole was shown in (1) of drawing 7 . As shown in (1) of drawing 7 , the case where epitaxial growth of the InAs is carried out on a GaAs substrate is the example. InAs grows epitaxially alternatively into the part of a hole and it becomes a quantum dot.
[0044] The case where it grew epitaxially alternatively in addition to the part of a hole was shown in (2) of drawing 7 . As shown in (2) of drawing 7 , the case where GaAs is grown up on a GaAs substrate is the example. GaAs grows up to be the other part alternatively, without growing up to be the part of a hole.
[0045] Besides the above, there are directions of the semi-conductor substrate of this invention. Recently, the anodization method is used as a micro-processing method of a semi-conductor. If this technique is used, the vesicular structure which consists of a hole of a high aspect ratio which has the path of nm size can be made easily. However, the location of a hole is random and fluctuation of the path of a hole is large under the effect. If the location of a hole is arranged regularly, it will be thought that the path of a hole becomes uniform. The location of a hole is formed in the place where electric field became large locally with irregularity with a detailed front face. If a hole is beforehand formed in a front face, increase of local electric field will take place in the part of a hole, and the hole of a high aspect ratio will be formed in the location. That is, if anodization of the semi-conductor substrate of this invention is carried out, anodization will advance from the part of a hole and the vesicular structure which consists of a hole of a high aspect ratio which takes a regular array will be obtained.
[0046] Although the above explanation was explained taking the case of compound semiconductors, such as GaAs and InP, it cannot be overemphasized that it is not restricted to this and can apply also with elemental semiconductors, such as Si and germanium.
[0047]
[Effect of the Invention] Since the low dry etching method of ingredient selectivity is used for this invention, etching progresses so that the configuration of the heights of the mold imprinted by the resist film may be maintained, and the detailed pattern with which the configuration of the heights of mold was reflected is formed in a semi-conductor front face.

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[Translation done.]

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]
[Drawing 1] It is drawing explaining the detailed pattern formation approach of this invention.
[Drawing 2] It is drawing showing the relation between the configuration of the heights formed in mold, and the configuration of the hole formed in the semi-conductor front face.
[Drawing 3] It is the mimetic diagram of a semi-conductor substrate which had the detailed pattern formed.
[Drawing 4] It is drawing showing the example of a detailed pattern.
[Drawing 5] It is drawing showing the example of the configuration of a hole.
[Drawing 6] It is drawing explaining the detailed pattern formation approach of this invention.
[Drawing 7] It is drawing explaining the use gestalt of this invention.
[Drawing 8] It is drawing explaining the conventional detailed pattern formation approach.

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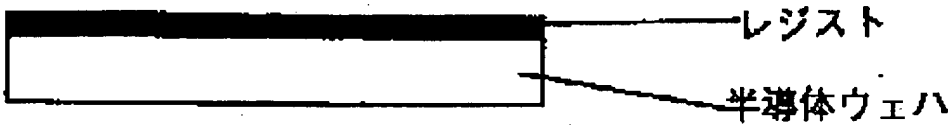
[Translation done.]

図1


(1) SiC製モールドの準備

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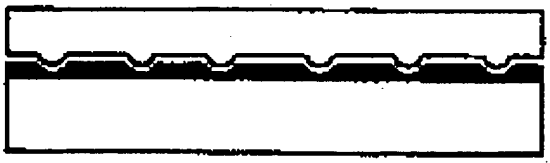

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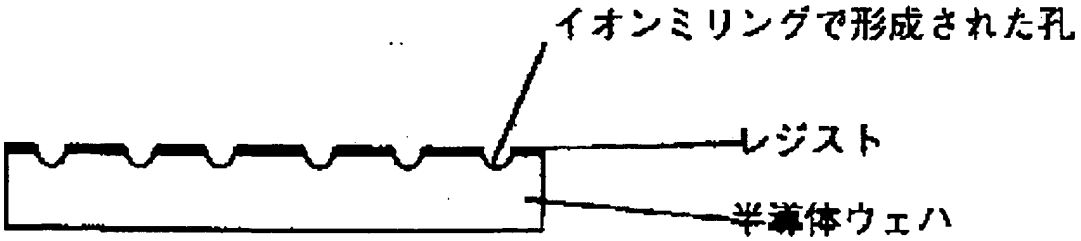


(4) イオンミリング

(5) レジストの除去

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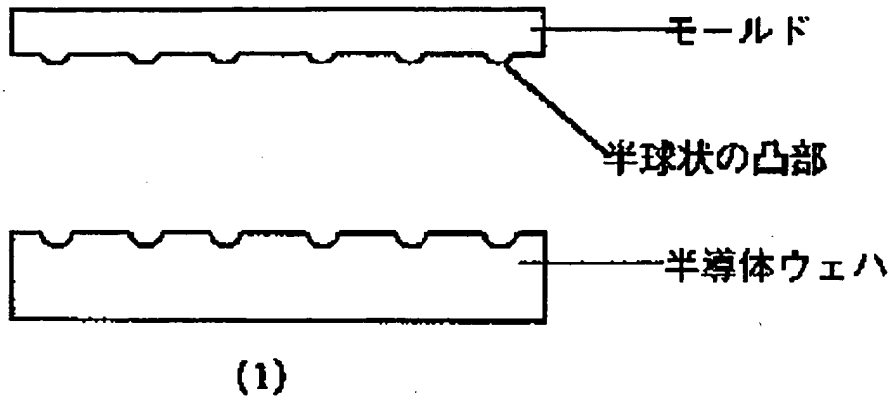


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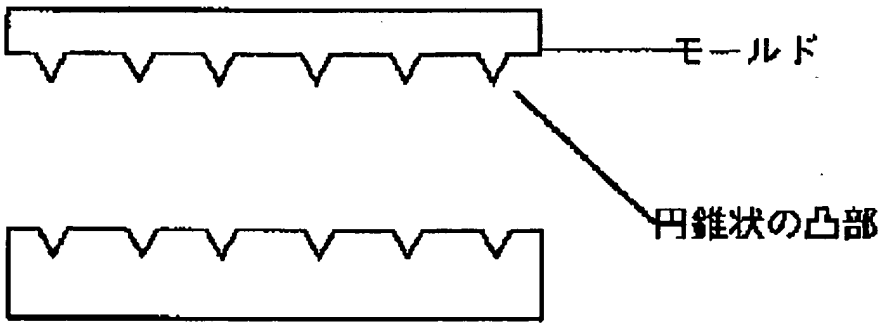


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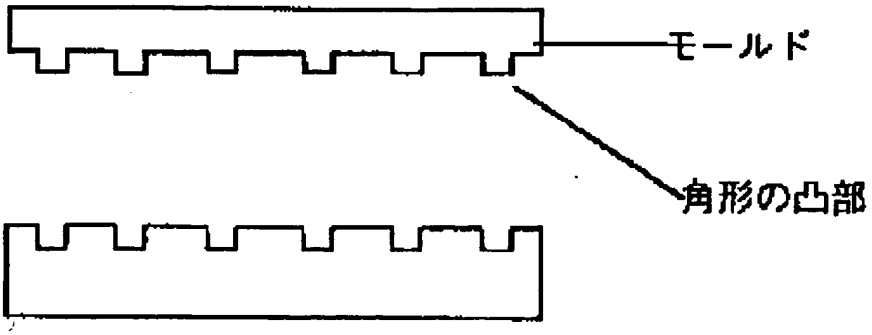


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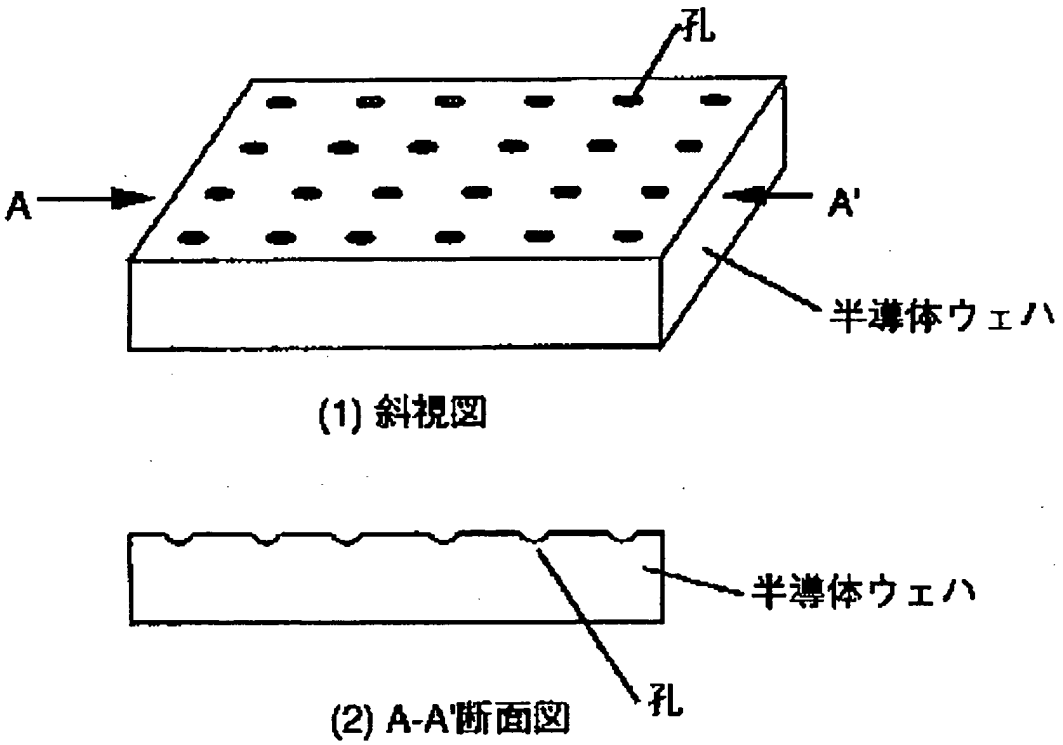

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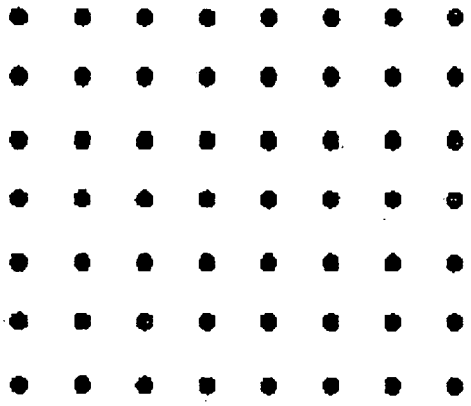

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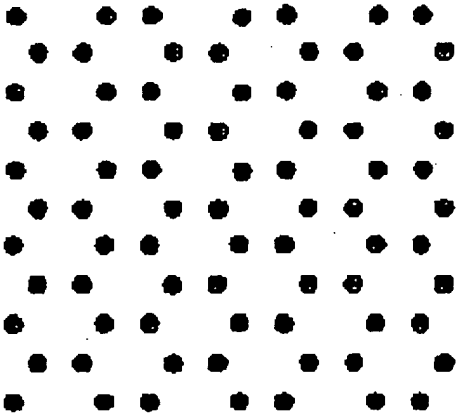

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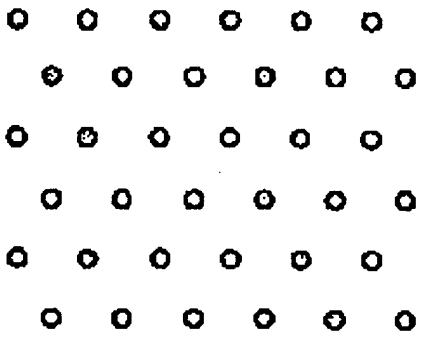

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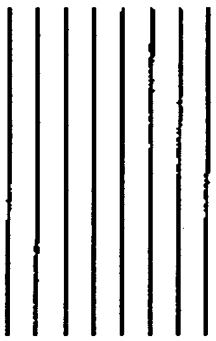

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図5

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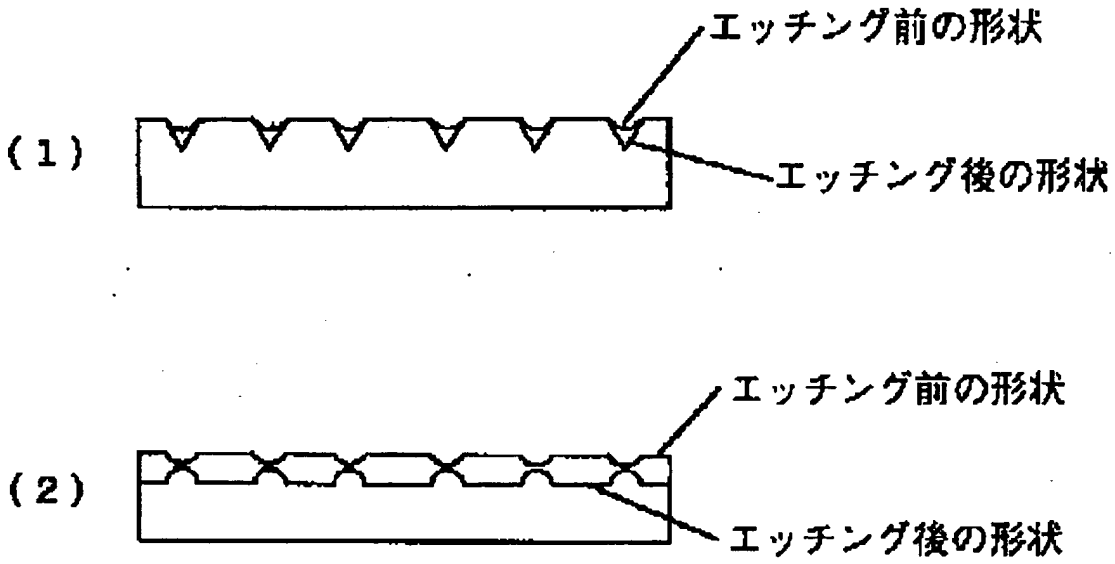
図6



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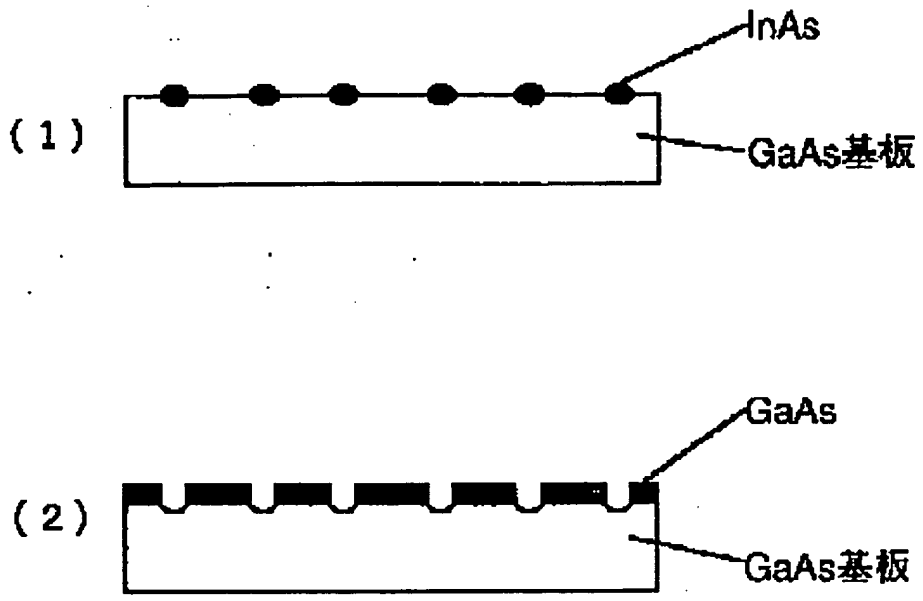

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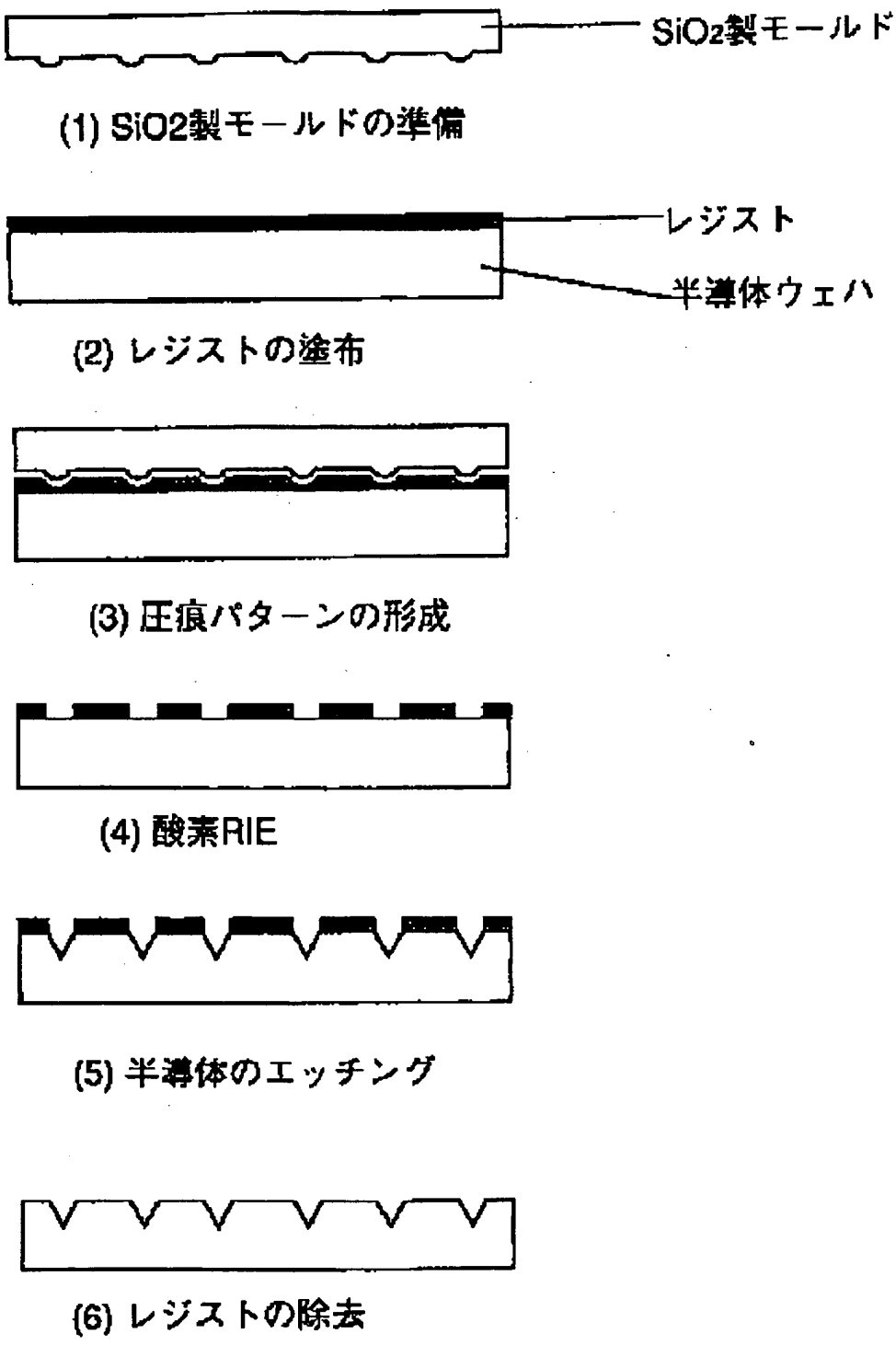
SiO2製モールド
(1) SiO2製モールドの準備
レジスト
半導体ウェハ
(2) レジストの塗布
(3) 圧痕パターンの形成
(4) 酸素RIE
(5) 半導体のエッチング
(6) レジストの除去